CLAIMS

We Claim:

1. An apparatus comprising:

a controller to generate command signals to a device to access the device to transfer data between the device and a bus coupled to the device; and

a flag signal generation unit to generate a flag signal to the device to trigger the data transfer between the device and the bus in response to a state transition that occurs in the flag signal after a specified period following a data transfer command, but said flag signal to also initiate a different command than the data transfer command in response to a state transition that occurs in the flag signal within the specified clock period.

2. The apparatus of claim 1 wherein the data transfer command is a read or write command and the different command is a precharge command.

3. The apparatus of claim 2 wherein the device is a memory device.

4. The apparatus of claim 1 wherein the memory device is a dynamic-random-access-memory, DRAM, which responds to a read or a write command to perform a corresponding data transfer between the DRAM and the bus if the flag signal has a transition after the lapse of a specified clock period, but first performs an auto-precharge on at least one bit line of the DRAM selected for the read or the write command if the flag signal has a transition within the specified clock period following the read or the write command.

5. The apparatus of claim 4 wherein the specified clock period is one clock period following the data transfer command.

6. An apparatus comprising:

a memory array to couple to a data bus to transfer data between said memory array and bus in response to a command signal received to initiate the data transfer; and

a timing unit coupled to receive the command signal to initiate the data transfer and also coupled to receive a flag signal to trigger the data transfer, said timing unit to interpret the flag signal to determine if the flag signal has a transition prior to a lapse of a specified clock period following the command signal and to perform a different command operation than data transfer, if the flag signal has a transition prior to the lapse of the specified clock period following the command signal.

7. The apparatus of claim 6 wherein the command signal is to perform a read or write operation and the different command operation is a precharge operation.

8. The apparatus of claim 6 wherein said timing unit generates an internal flag signal to trigger the data transfer if a transition of the flag signal occurs after the specified clock period following the command signal, but to generate an auto-precharge signal if a transition of the flag signal occurs prior to the lapse of the specified clock period following the command signal.

9. The apparatus of claim 8 wherein the command signal is to perform a read or write operation and the different command operation is an auto-precharge operation.

10. The apparatus of claim 9 further including a decoder coupled to the memory array to decode the command signal and at least one control circuit to perform the data transfer between said memory array and the data bus.

11. The apparatus of claim 10 wherein the apparatus is a dynamic-random-access-memory, DRAM.

12. The apparatus of claim 10 wherein the specified clock period is one clock period following the data transfer command.

13. A system comprising:

a controller to generate a data transfer command signal to effect data transfer and also to generate a flag signal to time triggering of the data transfer;

a memory device coupled to said controller to receive the data transfer command signal and transfer data in response to the data transfer command signal;

a bus coupled to said memory device to transfer data between said memory and bus in response to the data transfer command signal;

said controller to generate the flag signal to the memory device to trigger the data transfer between the memory device and the bus in response to a state transition that occurs in the flag signal after a specified clock period following the data transfer command signal, but said flag signal to also initiate a different command signal than the data transfer command signal in response to a state transition that occurs in the flag signal within the specified clock period; and

said memory to receive and interpret the flag signal to determine if the flag signal has a transition within the specified clock period following the command signal and to perform a different command operation from data transfer, in response to a transition present in the specified clock period following the data transfer command signal.

14. The system of claim 13 wherein said memory device is a dynamic-random-access-memory, DRAM.

15. The system of claim 14 wherein the different command signal is a precharge command.

16. The system of claim 13 wherein the data transfer command is a read or write command and the different command is an auto-precharge command associated with the read or write command.

17. The system of claim 16 wherein said controller is a memory controller.

18. The system of claim 16 further comprising a processor, wherein said controller is a memory controller coupled to said processor.

19. A method comprising:

issuing a command signal;

generating a flag signal in response to the issuing of the command signal to trigger a response to a corresponding operation of the command signal after a lapse of a specified time period following the issuing of the command signal; and

coding a different command on the flag signal by having the flag signal transition within the specified time period following the issuing of the command signal to perform a different operation than the corresponding operation of the command signal.

20. The method of claim 19 further comprising receiving the command and flag signals and interpreting the flag signal to determine if a transition is present within the specified time period following the issuing of the command signal.

21. The method of claim 20 wherein the different operation of the different command signal is a precharge operation of a memory.

22. The method of claim 20 wherein the command signal issues a read or write command to memory to perform a read or write operation.

23. The method of claim 22 wherein the different operation of the different command signal is an auto-precharge operation, which is performed prior to performing the read or write operation.

24. The method of claim 23 wherein the command and flag signals, including the coding of the different command signal in the flag signal, are issued to a dynamic-random-access-memory, DRAM.